10. A static logic to dynamic logic interface, comprising:

a clock that is the inverse of a second clock that causes dynamic logic to evaluate;

a delay element that generates a delayed clock; and,

a latch having a data input that interfaces to static logic, ~~and~~ an output that interfaces to dynamic logic, ~~and~~ a first pass gate having a first pass gate output, said first pass gate receiving said data input and being controlled by said delayed clock, ~~and~~ a second pass gate having a second pass gate output that controls a latching node of said latch, said second pass gate receiving said first pass gate output and being controlled by said ~~clock.~~

11. The interface of claim 10 wherein said latch inverts said latching node of said latch to produce said output.

IN THE ABSTRACT:

PLEASE RE-WRITE THE ABSTRACT AS FOLLOWS:

A static logic signal to dynamic logic interface that produces a monotonic output. An inverse of a dynamic logic evaluate clock is fed to the clock input of a transparent latch with clock and enable inputs. A delayed version of the inverse of the evaluate clock is generated by a delay element. The delayed inverse of the evaluate clock is fed to the enable input of the latch. The input to the latch comes from static logic and the output of the latch is fed to the dynamic logic. The net result is a latch that is open until the evaluate clock is instructing the dynamic logic to evaluate, and remains closed until a delay element delay time after the evaluate clock instructs the dynamic logic to reset.